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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/091,262 | 03/05/2002 | Steven L. Stewart | USA/01/012 | 6437 |

33249 7590 08/24/2004

RESOLUTION PERFORMANCE PRODUCTS LLC
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| EXAMINER | |
|---|---|
| CHANG, VICTOR S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1771 | |

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/091,262 | STEWART ET AL. | |
| | Examiner | Art Unit | |
| | Victor S Chang | 1771 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-6,8-28 and 62-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-28 and 62-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

**1.** The Examiner has carefully considered Applicants' amendments and remarks filed on 7/2/2004. Applicants' amendments to claim 1 has been entered.

**2.** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

**3.** Rejections not maintained are withdrawn.

### *Claim Rejections - 35 USC § 102*

**4.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**5.** Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 08250835 (computer translation).

It is noted that newly amended claim 1 has deleted the complex viscosity property of the thermoplastic adhesive, and the temperature at which the thermoplastic adhesive is a solid or semi-solid.

JP 08250835 is directed to a method of connecting a LSI package having metallic bumps (a surface mount electronic device) to a printed wiring board (printed circuit board) with an intermediate film-like sheet of an organic resin having a melting

point and coefficient of thermal expansion about the same as the metallic bumps (i.e., a thermoplastic adhesive as the intermediate layer). The method improves the reliability of the connection (Abstract). JP '835 also expressly teaches that examples of LSI package include a BGA mold LSI package and a flip chip mold package (paragraph 0001), which reads on the element "encapsulated integrated circuit mounted on a connecting substrate having a bottom surface" of amended claim 1. Furthermore, the Examiner notes that Fig. (a) also clearly shows a molded (encapsulated) LSI package.

For claims 1, 3 and 4, JP '835 teaches all the elements as claimed. Claims lack novelty.

**6.** Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP 08250835 (Abstract) in view of Mohri et al. (US 6132543).

The teachings of JP '835 are again relied upon as set forth above.

For claim 5, JP '835 lacks an express teaching of the function of the surface mounted electronic device. However, it is noted that Mohri's invention is directed to a method of manufacturing a packaging substrate, and Mohri teaches that it is known art that the BGA type packages are most suitable for further miniaturization of packages especially for LSI's which dissipate a large quantity of heat due to high speed signal transmission in devices such as microprocessors (column 1, lines 19-25). As such, in the absence of unexpected results, it is the Examiner's position that incorporating a microprocessor LSI in the method of JP '835 is either anticipated, or an obvious selection to one of ordinary skill in the art, motivated by the desire to improve the reliability of the connection.

**7.** Claims 6, 8-22 and 62-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 08250835 (Abstract) in view of Schrock et al. (US 6541872), substantially for the reasons set forth in section 4 of Office action dated 4/28/2004, together with the following additional observations.

It is noted that newly amended claim 1 now recites, *inter alia*, "an encapsulated integrated circuit mounted on a connecting substrate having a bottom surface, wherein the surface mount electronic device is attached to a printed circuit board."

Applicants' arguments "applicants have amended claim 1 to further clarify that the surface mount device of the present invention is pre-manufactured and encapsulated" (Remarks, page 9, 4th paragraph) and "Both Schrock and JP '835 are directed to manufacturing a die package" (Remarks, page 10, first full paragraph) have been carefully considered, but is not persuasive. The Examiner notes that JP '835 expressly teaches that examples of LSI package include a BGA mold LSI package and a flip chip mold package (paragraph 0001), which reads on the newly added element "encapsulated integrated circuit mounted on a connecting substrate having a bottom surface", as set forth above, Applicants' argument to the contrary notwithstanding.

## ***Conclusion***

**8.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor S Chang whose telephone number is 571-272-1474. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Terrel H Morris can be reached on 571-272-1478. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VSC
Victor S Chang
Examiner
Art Unit 1771

8/11/2004

TERREL MORRIS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700